# SAMPLE QUESTION PAPER FOR END SEMESTER EXAMINATION(KT)

**September 2020**

**SEM VI** **SUBJECT: VLSI Design**

**Max Marks: 50**

- **Answer all Questions**
- **Figures to the right indicate marks assigned**

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1. **When no Gate Signal is applied to a MOSFET;** **[1]**
   a. High ***R*** exist between Source and Drain and no current flows
   b. Two Back-to-Back Diodes exist in Series between Drain and Source
   c. Both a. and b.
   d. A Channel is Created between Source and Drain
2. **For a small value of $V_{DS}$ the channel in MOSFET is;** **[1]**
   a. a. Not formed b. a linear resistor whose value is controlled by $V_{GS}$.
   b. c. Pinched off d. Enhanced
3. **Smallest Size Digital Logic Inverter is;** **[1]**
   a. a. BJT Based b. Diode Based
   b. c. CMOS Based d. Amplifier Based
4. **_____ is about twice as fast as P-MOS.** **[1]**
   a. CMOS b. DMOS c. MOD d. N-MOS
5. **The time it takes for an input signal to pass through internal circuitry and generate the appropriate output effect is known as _____.** **[1]**
   a. fan-out b. propagation delay c. rise timed. fall time

**7. Speed power product is measured as the product of…..** **[1]**

a) gate switching delay and gate power dissipation

b) gate switching delay and gate power absorption

c) gate switching delay and net gate power

d) gate power dissipation and absorption

**8. Source and drain in nMOS device are isolated by….** **[1]**

a) a single diode b) two diodes

c) three diodes d) four diodes

**9. The condition for non conducting mode is** **[1]**

a) Vds lesser than Vgs b) Vgs lesser than Vds

c) Vgs = Vds = 0 d) Vgs = Vds = Vs = 0

**10. nMOS is** **[1]**

a) donor doped b) acceptor doped

c) all of the mentioned d) none of the mentioned

**11. MOS transistor structure is** **[1]**

a) symmetrical b) non symmetrical

c) semi symmetrical d) pseudo symmetrical

**12.As source drain voltage increases, channel depth** **[1]**

a) increases b) decreases

c) logarithmically increases d) exponentially increases

**13. If p-transistor is conducting and has small voltage between source and drain, then the it is said to work in** **[1]**

a) linear region b) saturation region

c) non saturation resistive region d) cut-off region

**14. Mobility depends on** **[1]**

a) transverse electric field b) Vg

c) Vdd d) Channel length

**15. NOR type flash allows _____ to be read or written independently** **[1]**

a) one machine cycle b) one machine word

c) one machine sentence d) one bit

**16. NAND type flash memories are used in** **[1]**

a) memory cards b) USB

c) solid state drivers d) all of the mentioned

**17. The transistors in NAND type flash are connected in** **[1]**

a) series b) parallel c) cascade d) randomly

**18. The program erase cycle in flash memory is** **[1]**

a) finite b) infinite c) all of the mentioned d) none of the mentioned

**19.** In Pseudo-nMOS logic, n transistor operates in **[1]**

a) cut off region
b) saturation region
c) resistive region
d) non saturation region

**20. The power dissipation in Pseudo-nMOS is reduced to about _____ compared to nMOS device.** **[1]**

a) 50%
b) 30%
c) 60%
d) 70%

**21. Pseudo-nMOS has higher pull-up resistance than nMOS device.** **[1]**

a) true
b) false

**22. In dynamic CMOS logic _____ is used.** **[1]**

a) two phase clock
b) three phase clock
c) one phase clock
d) four phase clock

**23. In clocked CMOS logic, output in evaluated in** **[1]**

a) on period
b) off period
c) both periods
d) half of on period

**24. In clocked CMOS logic, rise time and fall time are** **[1]**

a) faster
b) slower
c) faster first and then slows down
d) slower first and then speeds up

**25. Clocked sequential circuits are** **[1]**

a) two phase overlapping clock
b) two phase non overlapping clock
c) four phase overlapping clock
d) four phase non overlapping clock

**26. When both nMOS and pMOS transistors of CMOS logic gates are ON, the output is:** [1]

a) 1 or Vdd or HIGH state
b) 0 or ground or LOW state
c) Crowbarred or Contention(X)
d) Less than Vdd

**27. For carry skip adder, the minimum total propogation delay can be obtained when m is** **[1]**

a) sqrt(nk1/k2)
b) sqrt(2nk1/k2)
c) sqrt(2k1/nk2)
d) sqrt(nk1k2/2)

**28. Multiple output domino logic has** **[1]**

a) two cell manchester carry chain
b) three cell manchester carry chain
c) four cell manchester carry chain
d) four cell manchester carry look ahead

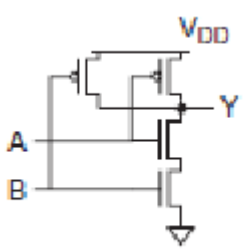
**29. Which method uses reduced number of partial products?** **[1]**

a) Baugh-wooley algorithm
b) Wallace trees
c) Dadda multipliers
d) Modified booth encoding

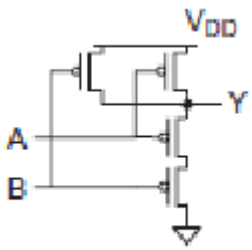
**30. Which method is easier to manipulate accumulator content?** **[1]**

a) left shifting
b) right shifting
c) serial shifting
d) parallel shifting

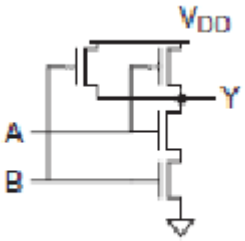
**31. The CMOS logic circuit for NAND gate is:** **[2]**



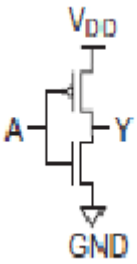

**a.**




**b.**




**c.**




**d**

**32. What type of logic gate's behaviour does this truth table represent?** **[2]**

| ? | | | |
|---|---|---|---|
| A | B | C | ? |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

a.2 input OR b. 3 input OR c. 3 input EXOR d. 4 input EXOR

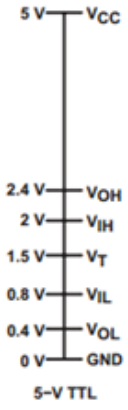
**33. How many bits must each word have in one-to-four line de-multiplexer to be implemented using a memory?** **[2]**

a) 8 bit b)4 bits c)2 bits d)1 bits

**34. A full Adder has….** **[2]**

a) 2 inputs, 2 outputs
b) 2 inputs, 1 output
c) 3 inputs, 2 outputs
d) 3 inputs, 1 output

**35.** Determine the Noise Margin for 5V TTL inverter gate: **[2]**




a) NMH = 0.4V and NML =0.4V
b) NMH = 2.4V and NML = 0.4V
c) NMH = 2V and NML = 0.8V
d) NMH = 1.5V and NML = 0.4V

**36. The switching threshold voltage VTH for an ideal inverter is equal to:** **[2]**

a) (VDD-VOL)/2

b) VDD

c) (VDD)/2

d) 0

**37. In VLSI design, which process deals with the determination of resistance & capacitance of interconnections?** **[2]**

**a.** Floorplanning

**b.** Placement & Routing

**c.** Testing

**d.** Extraction

**38. The output of sequential circuit is regarded as a function of time sequence of _____.** **[2]**

**A. Inputs B. Outputs C. Internal States D. External States**

**a. A & D**

**b. A & C**

**c. B & D**

**d. B & C**

**39. Which method/s of physical clocking is/are a /the recursive structure where the memory elements are grouped together to make the use of nearby or same distribution points?** **[2]**

a. H tree

b. Balanced tree clock network

c. Random Tree

d. I tree

**40. For a pseudo nMOS design the impedance of pull up and pull down ratio is** **[2]**

a) 4:1

b) 1:4

c) 3:1

d) 1:3

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**Note: These Questions are only for display purpose**