SAMPLE QUESTION PAPER FOR END SEMESTER EXAMINATION(KT)

September 2020

SEM VI **SUBJECT: DLIC** **Max Marks: 50**

(Q.1 to 16 carry one mark and Q.17to 33 carry 2 marks)

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1. Which is not the internal circuit of operational amplifier?
   a) Differential amplifier b) Level translator
   c) Output driver d) Clamper
2. The purpose of level shifter in Op-amp internal circuit is to
   a) Adjust DC voltage b) Increase impedance
   c) Provide high gain d) Decrease input resistance
3. How a symmetrical swing is obtained at the output of Op-amp
   a) Providing amplifier with negative supply voltage
   b) Providing amplifier with positive voltage
   c) Providing amplifier with positive& negative voltage
   d) None of the mentioned
4. What is the purpose of differential amplifier stage in internal circuit of Op-amp?
   a) Low gain to differential mode signal
   b) Cancel difference mode signal
   c) Low gain to common mode signal
   d) Cancel common mode signal
5. Which of the following is not preferred for input stage of Op-amp?
   a) Dual Input Balanced Output
   b) Differential Input Single ended Output
   c) Cascaded DC amplifier
   d) Single Input Differential Output
6. To reduce the output offset voltage V_{ooT} to zero
   a) Input offset voltage compensating network is added at the inverting input terminal
   b) Input offset voltage compensating network is added at the non-inverting input terminal
   c) Input offset voltage compensating network is added at the output terminal
   d) None of the mentioned
7. Why does an op-amp without feedback is not used in linear circuit application?
   a) Due to high current gain b) Due to high voltage gain
   c) Due to high output signal d) All of the mentioned
8. When the input voltage is reduced to zero in a closed loop configuration the circuit acts as
   a) Inverting amplifier b) Non-inverting amplifier
   c) Inverting and non-inverting amplifier d) None of the mentioned
9. How the value of output offset voltage is reduced in closed loop op-amp?
   a) By increasing gain b) By reducing gain
   c) By decreasing bandwidth d) By reducing bandwidth
10. Common mode voltage gain of an op-amp is generally
    a) >1 b) =1 c) <1 d) 0
11. Define the common-mode rejection ratio (CMRR) of op-amp?
    a) CMRR=A_D/A_{CM} b) CMRR=A_{CM}/ A_D
    c) CMRR=V_{OCM}/A_{CM} d) CMRR=A_D*A_{CM}

12. Higher value of common mode rejection ratio can be reached
    a) By reducing the common mode voltage b) By decreasing the differential gain
    c) By reducing the common mode input voltage d) All of the mentioned
13. What happens when the operating frequency of an op-amp increase?
    a) Gain of the amplifier decrease b) Phase shift between output and input signal decrease
    c) Gain and phase shift of amplifier decreases d) Gain becomes '0'
14. Measure taken to increase the bandwidth of an op-amp.
    a) Increase the frequency for the configuration b) Reduce the gain of the configuration
    c) Closed loop configuration is used d) Open loop configuration is used
15. Slew rate is defined as the rate of change of
    a) Output voltage with respect to time b) Input voltage with respect to time
    c) Both output input voltage with respect to time d) None of the mentioned
16. Which factor is responsible for causing slew rate?
    a) Internal capacitor b) External resistor
    c) None of the mentioned d) Both internal and external capacitor
17. Calculate the time taken by the output to swing from +14v to -14v for a 741C op-amp having a slew rate of 0.5V/µs?
    a) 22µs b) 42µs c) 56µs d) 70µs
18. Determine the expression of output voltage for inverting summing amplifier consisting of four internal resistors? (Assume the value of internal resistors to be equal)
    a) $V_o = -(R_f/R)\times(V_a + V_b + V_c + V_d)$ b) $V_o = (R_F/R)\times(V_a + V_b + V_c + V_d)$
    c) $V_o = (R/R_F)\times(V_a + V_b + V_c + V_d)$
19. An inverting summing amplifier with gain 1 have different input voltages: 1.2v,3.2v and 4.2v. Find the output voltage?
    a) 4.2v b) 8.6v c) -4.2v d) -8.6v
20. Find the output voltage of the integrator
    a) $V_o = -(1/R\times C_F)\times \int_0^t V_{in}dt + C$ b) $V_o = (R/C_F)\times \int_0^t V_{in}dt + C$
    c) $V_o = (C_F/R)\times \int_0^t V_{in}dt + C$ d) $V_o = (R\times C_F)\times \int_0^t V_{in}dt + C$
21. Determine the output voltage of the differentiator?
    a) $V_O = R_F\times C_1\times[dV_{in}/dt]$. b) $V_O = -R_F\times C_1\times[dV_{in}/dt]$. c) $V_O = R_F\times C_F\times[dV_{in}/dt]$.
22. The gain of the first order low pass filter
    a) Increases at the rate 20dB/decade b) Increases at the rate 40dB/decade
    c) Decreases at the rate 20dB/decade d) Decreases at the rate 40dB/decade
23. Determine the expression for output voltage of first order high pass filter?
    a) $V_O = [1+(R_F/R_1)]\times[(j2\pi fRC/(1+j2\pi fRC)] \times V_{in}$
    b) $V_O = [-(R_F/R_1)]\times[(j2\pi fRC/(1+j2\pi fRC)] \times V_{in}$
    c) $V_O = \{[1+(R_F/R_1)]\times/[1+j2\pi fRC]\}\times V_{in}$
24. Determine voltage gain of second order high pass butterworth filter.
    Specifications $R_3 = R_2 = 33\Omega$, f=250hz and f_L=1khz.
    a) -11.78dB b) -26.51dB c) -44.19dB d) 11.78dB
25. The number of comparators required for flash type A/D converter
    a) Triples for each added bit b) Reduce by half for each added bit
    c) Double for each added bit d) Doubles exponentially for each added bit
26. Calculate the conversion time of a 12-bit counter type ADC with 1MHz clock frequent to convert a full scale input?
    a) 4.095 µs b) 4.095ms c) 4.095s d) 4.5ms
27. A dual slope has the following specifications:
    16bit counter; Clock rate =4 MHz; Input voltage=12v; Output voltage =-7v and Capacitor=0.47µF.If the counters have cycled through 2^n counts, determine the value of resistor in the integrator.
    a) 60kΩ b) 50kΩ c) 120kΩ d) 100kΩ

28. Find out the resolution of 8 bit DAC/ADC?
    a) 562 b) 625 c) 256 d) 265

29. Sample and hold circuit are used in
    a) Analog to Digital modulation
    b) Digital to analog modulation
    c) Pulse position modulation
    d) All of the mentioned
30. Determine the time period of a monostable 555 multivibrator.
    a) T = 0.33RC b) T = 1.1RC
    c) T = 3RC d) T = RC
31. A monostable multivibrator has R = 120kΩ and the time delay T = 1000ms, calculate the value of C?
    a) 0.9µF b) 1.32µF c) 7.5µF d) 2.49µF
32. Astable multivibrator operating at 150Hz has a discharge time of 2.5m. Find the duty cycle of the circuit.
    a) 50% b) 75% c) 95.99% d) 37.5%
33. What is the function of low pass filter in phase-locked loop?
    a) Improves low frequency noise
    b) Removes high frequency noise
    c) Tracks the voltage changes
    d) Changes the input frequency

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THESE ARE SAMPLE QUESTIONS FOR DISPLAY PURPOSE ONLY