ELEX ESE Regular (VIIIth Sem/ CBCGS-H) October2020
AMVD/SEM VIII(CBCGS-H)
EXC802: SAMPLE QUESTION SET for Analog Mixed VLSI Design

Max Marks: 50

- **Answer all Questions**
- **Figures to the right indicate marks assigned**

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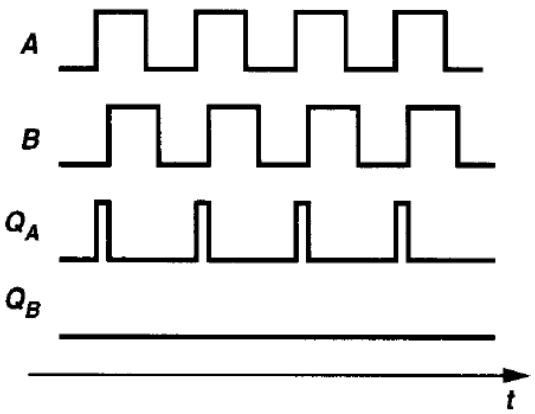
1. The PLLs where frequency detection is aided with phase detection is known as

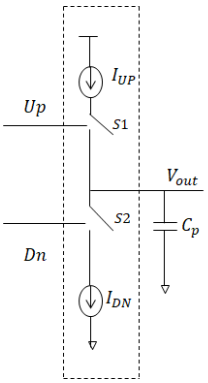
a. Type I PLL
b. Charge Pump PLL
c. Simple PLL
d. Type II PLL

2. For a PFD, the figure below shows



a. Frequency A leads B
b. Frequency B leads A
c. Frequency A and B are equal
d. Frequency A lags B

3. The circuit below represents



a. Phase frequency Detector
b. Phase Detector
c. Charge Pump
d. Low pass filter

4.. Which of the following statements are true?
a. The substrate of NMOS should have potential more than that of source or drain.
b. The substrate of NMOS should have the lowest potential.
c. The substrate of PMOS should have the highest potential.
d. None of the above.

5. Which of the following statements are true ?
a. The source-bulk junction should be forward-biased.
b. The source-bulk junction should be reverse-biased.
c. The drain-bulk junction should be reverse-biased.
d. The drain-bulk junction should be forward-biased.

6. The zero crossing points of the VCO output experience substantial random variations called as

a. Ripple
b. Skew
c. Dead Zone
d. Jitter

7. The zero crossing points of the VCO output experience substantial random variations called as

a. Phase error
b. Skew
c. Dead Zone
d. Jitter

8. PFDs exhibit small or zero gain near the phase lock known as

a. Dead Zone
b. Current Mismatch
c. Missing edge phenomenon
d. Timing Mismatch

9.. Which of the following statements are true ?
a. For NMOS, as VSB increases, threshold voltage increases.
b. For NMOS, as VSB increases, threshold voltage decreases.
c. For PMOS, as VSB increases, threshold voltage increases.
d. For PMOS, as VSB increases, threshold voltage decreases.

10. Which of the following statements are true ?
a. If gm increases, gmb increases.
b. For NMOS as VSB increases, gmb decreases.
c. For PMOS as VSB increases, gmb decreases.
d. All of the above.

11. The range of input signal frequencies over which the loop can maintain the lock is called as

a. Acquisition Range
b. Lock Range
c. Tracking Range
d. Pull in Range

12. The range of input signal frequencies over which PLL can acquire a lock is called as

a. Capture Range
b. Lock Range
c. Tracking Range
d. Pull in Range

13. Magnitude difference between charging and discharging currents is known as

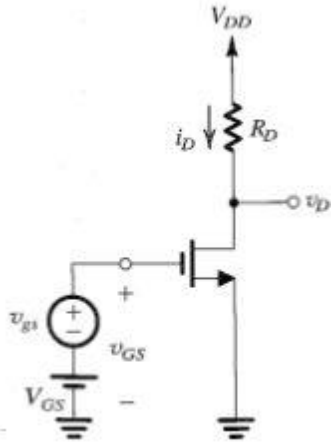
a. Charge Sharing
b. Current Mismatch
c. Clock Feedthrough
d. Timing Mismatch

14. In dual slope type of ADCs, an input hold time is _____.

a. Almost zero
b. Higher than that of flash type ADCs
c. Longest
d. Lowest

15. Which capacitance in MOSFET is mainly responsible for limiting the frequency of operation?
a. CGS
b. CSD
c. CGD
d. CGG

16. Consider the FET amplifier given below. Threshold voltage = 2 V, k'W/L = 1 mA/V2, VGS = 4 V, VDD = 10 V, and RD = 3.6 kohm.



a. What are the DC quantities ID and VD?
a. 2 mA, 7.2 V
b. 1 mA, 10 V
c. 2 mA, 2.8 V
d. 200 mA, 2.8 V

b. What is the value of gm at the bias point?
a. 1 mA/V
b. 2 mA/V
c. 4 mA/ V
d. 5 mA/V

c. What is the voltage gain?
a. 3.6

b. 7.2
c. -3.6
d. -7.2 29.

d. If \lambda = 0.01 V-1, what is the output resistance at the bias point?
a. 25 kohm
b. 40 kohm
c. 50 kohm
d. 100 kohm

e. Taking into consideration the output resistance, what is the voltage gain?
a. 6.7
b. 7.2
c. -6.7
d. 3.6

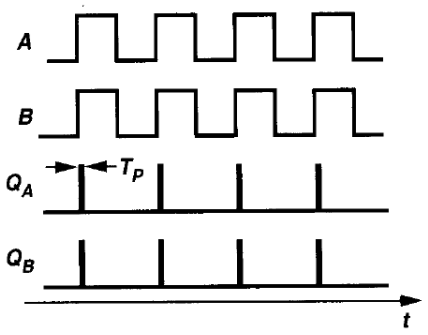
17. The non-idealities of PFD results in

A. Phase error
B. Reference Spur
C. Jitter

a. A and B
b. A and C
c. B and C
d. A,B and C

18.For signals A and B with zero phase difference what will be the pulses generated for $Q_A$and Q_B?

a.



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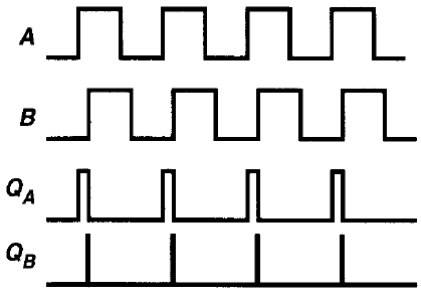

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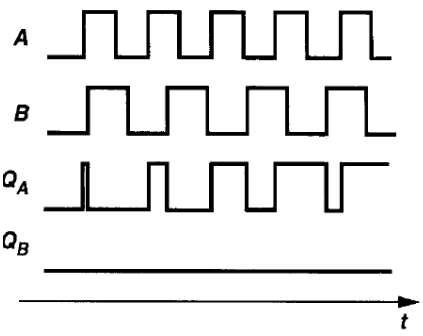

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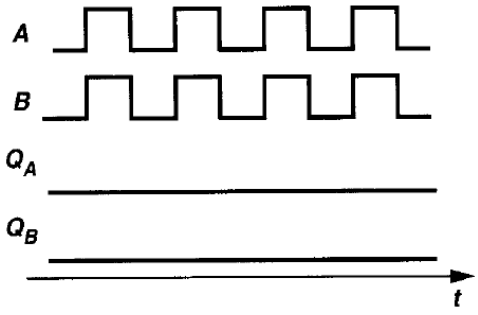


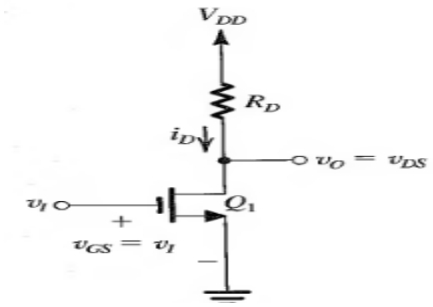
19. Current sources in CP circuit are implemented using

a. Current Amplification circuits
b. Current Divider circuits
c. Current Mirror circuits
d. Current reduction circuits

20.The difference between analog voltage represented by two adjacent digital codes, or the analog step size, is called the
a. Quantization
b. Accuracy
c. Resolution
d. Monotonicity

Sample-and-hold circuits in analog-to digital converters (ADCs) are designed to
a. Sample and hold the output of the binary counter during the conversion process
b. Stabilize the comparator's threshold voltage during the conversion process
c. Stabilize the input analog signal during the conversion process
d. Sample and hold the D/A converter staircase waveform during the conversion process

21 Consider the amplifier below for the case VDD = 5 V, RD = 24 kΩ, (W/L) = 1 mA/V2, and Vt = 1 V.



22 If the amplifier is biased to operate with an overdrive voltage VOV of 0.5 V, find the incremental gain at the bias point.
a) -3 V/V
b) -6 V/V
c) -9 V/V
d) -12 V/V

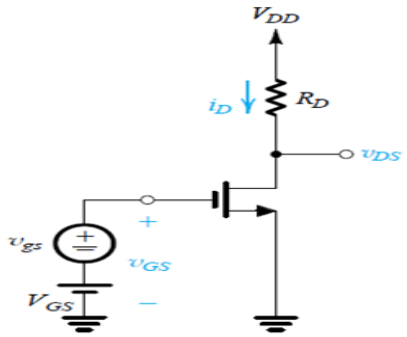
23. For amplifier biased to operate with an overdrive voltage of 0.5V, and disregarding the distortion caused by the MOSFET's square-law characteristic, what is the largest amplitude of a sine-wave voltage signal that can be applied at the input while the transistor remains in saturation?
a) 1.61 V
b) 1.5 V
c) 0.11 V
d) 3.11 V

24. For the input signal of 1.5V what is the value of the gain value obtained?
a) -12.24 V/V
b) -12.44 V/V
c) -12.64 V/V
d) -12.84 V/V

25.If the process transconductance parameter is 50μA/V2, what is the MOSFET's W/L?
a) 25
b) 50
c) 75
d) 100

26. Which of the following is the fastest switching device?
a) JEFT
b) Triode
c) MOSFET
d) BJT

27.Consider the amplifier circuit shown below. The transistor is specified to have Vt = 0.4 V, kn = 0.4 mA/V2, W/L = 10 and λ = 0. Also, let VDD = 1.8V, RD = 17.5kΩ, VGS = 0.6V and vgs = 0V.



28.Find ID.
a) 0.08 mA
b) 0.16 mA
c) 0.4 mA
d) 0.8 mA

29. Find VDS.
a) 0.1V
b) 0.2 V
c) 0.4 V
d) 0.8 V

30. Find Av.
a) -12 V/V
b) -14 V/V
c) -16 V/V
d) -18 V/V

30. The cut-off frequency (fβ) is basically the frequency at which the short circuit _____
a) CB gain of transistor drops by 3 dB from its value at low frequency
b) CE gain of transistor drops by 3 dB from its value at low frequency
c) CC gain of transistor drops by 3 dB from its value at low frequency
d) CC gain of transistor drops by 3 dB from its value at high frequency

31.What should be the level of input resistance to allow the occurrence of source loading in common base amplifier configuration?
a) Low
b) High
c) Moderate
d) Stable

32.A transconductance amplifier is also called _____
a) current to voltage convertor
b) voltage to current convertor
c) resistor
d) inductor

33. MOSFET from a JFET differs mainly because _____
a) of power rating
b) of the output
c) the JFET has a pn junction
d) the MOSFET has two gates

34. The voltage gain is practically expressed in _____
a) db
b) volts
c) as a number
d) ampere

35. Gain of an amplifier usually expressed in db because _____
a) It is a small unit
b) Calculations become easy
c) Human ear response is logarithmic
d) Gain is reduced

36.The total gain of a multistage amplifier is less than the product of the gains of individual stages due to _____
a) Power loss in the coupling device
b) Loading effect of the next stage
c) The use of many transistors
d) The use of many capacitors

37.The fF (E) decreases in which of the following band for p-type semiconductor?
a) Conduction band
b) Donor band
c) Acceptor band
d) Valence band

38. The displacement of the charges results in
a) Magnetic field

b) Electric field
c) Rust
d) Hall effect

39.What is the value of 1 micron?
a) 10-6cm
b) 10-5cm
c) 10-4cm
d) 10-3cm

40.Which of the following results when the equilibrium established in a semiconductor?
a) Restrain the process of diffusion
b) Electric field becomes very high
c) Restrain the process of diversion
d) Electric field becomes very Low

41.Convert 10 micron to meters.
a) 10-5m
b) 107m
c) 10-6m
d) 10-4m

42. The point on the DC load line which is represented by 'Q' is called _____
a) cut off point
b) cut in point
c) breakdown point
d) operating point

43. For which region of operation is a mosfet represented by its small signal model?
a. Triode
b. Saturation
c. Cut-off
d. Independent of the region

44. Channel length modulation is taken into consideration in the small signal model by:
a. Placing a resistor between gate and source
b. Placing a capacitor between gate and drain
c. Placing a resistor between source and drain
d. Placing a resistor between source and Bluk

45. Output resistance of a mosfet is:

a. Directly proportional to VGS
b. Independent of VGS
c. Inversely proportional to VGS
d. sometimes proportional to VGS .

46. For an ideal mosfet the output resistance is:
a. Zero
b. infinity
c. Of the order of tens of ohms
d. Of the order of hundreds of ohms.

47. The ratio of output current change against an input voltage change is called:
a. Trans-conductance
b. Siemens
c. Resistivity
d. Gain

48. For a MOSFET with trans-conductance gm = 1.5 mS, and input signal \deltaV = 2 mV, then
a. \deltaId = 3 \muA
b. \deltaId = 2 \muA
c. \deltaId = 1.5 \muA d. \deltaI
d = 0.75 \muA

49. during the measurement of output impedance:
a. Input voltage change = 0
b. Input current change = 0
c. Both input voltage change = 0 and input current change =0
d. None input voltage change = 0 and input current change =0.

50. During the measurement of input impedance:
a . Output current change = 0
b. Input current change = 0
c. Input voltage change = 0
d. Output voltage change = 0

51. While writing the small-signal model of a circuit:
a. DC voltage sources are retained
b. DC voltage sources are short circuited
c. Result does not get affected by the DC voltage sources
d. AC voltage sources are retained

52. While writing the small-signal model of circuit:
a. DC current sources are retained

b. DC current sources are short circuited
c. DC current sources are open circuited
d. AC voltage sources are retained.

53. For low frequency operations, input impedance at the gate of the mosfet can be approximated to be:
a. Zero
b. Of the order of ohms
c. Directly proportional to frequency
d. infinity.

54. The magnitude of the input impedance of a mosfet is:
a. Directly proportional to the frequency of operation
b. Independent of the frequency of operation
c. Inversely proportional to the frequency of operation
d. dependent of the frequency of operation.

55. Which of the following statements are true?
a. Body effect causes variation in threshold voltage.
b. The bulk-source potential causes the depletion layer width to change.
c. Body effect causes non variation in threshold voltage.
d. The bulk-source potential causes the depletion layer width to no change.

56. What is the trans-conductance of a MOSFET when \deltaID = 1 mA and \deltaVin = 1 V?
a. 1 kS
b. 1 mS
c. 1 kohm
d. 1 Mohm

57. The action of a MOSFET in its small signal model can best be represented as a:
a. Current controlled current source
b. Current controlled voltage source
c. Voltage controlled current source
d. Voltage controlled voltage source.

Consider a NMOS transistor having k'W/L = 2 mA/V2. Let the transistor be biased at VOV = 1 V. Now answer the questions
58. For operating in saturation mode, what is the bias current ID ?
a. 1 mA
b. 2 mA
c. 4 mA
d. 8 mA

59. If a +0.1 V signal is superimposed on VGS, find the corresponding increase in drain current ?
a. 1 mA

b. 2 mA
c. 1.21 mA
d. 0.21 mA

60. Use the result of question above to calculate gm.
a. 12.1 mA/V
b. 2.1 mA/V
c. 1 mA/V
d. 10 mA/V

61. If a -0.1 V signal is superimposed on VGS, find the corresponding decrease in drain current?
a. 1 mA
b. 0.81 mA
c. 0.19 mA
d. 0.5 mA

62.To calculate gm.
a. 19 mA/V
b. 1.9 mA/V
c. 1 mA/V
d. 0.5 mA/V

63. The equivalent weight of LSB in a four bit resistive divider ADC is

a. 1/4
b. 1/15
c. 1/16
d. 8/15