Microcontroller & Applications
Mock Paper for Sept 2020
TE SEM V CBCGS

Sr No	MCA ESA	Marks
	Multiple Choice Questions	
1	1.What is the address range of SFR Register bank?	1
	a)00H-77H	
	b)40H-80H	
	c)80H-7FH	
	d)**80H-FFH**	
2	2.Which pin of port 3 is has an alternative function as read control signal for	1
	a)P3.8	
	b)P3.3	
	c)P3.6	
	d)P3.7	
3	3.7.Which of the following is not an addressing mode of 8051?	1
	a)register specific instructions	
	b)register instructions	
	c)indexed	
	d)None of above	
4	4.The bits that control the external interrupts are	
	a)ET0 and ET1	
	b)ET1 and ET2	
	c)EX0 and EX1	
	d)EX1 and EX2	
5	5.ES bit is used to	
	a)enable or disable external interrupts	
	b)enable or disable internal interrupts	
	c)enable or disable all the interrupts	
	d)none of the mentioned	
6	6.This program code will be executed continuously:	2
	STAT:MOV A, # FFH	
	DJNZ STAT	
	a)True	
	b)False	
7	7.11.The internal RAM memory of the 8051 is:	
	a)32 bytes	
	b)64 bytes	
	c)128 bytes	
	d)256 bytes	
8	8.Program counter holds.....	1
	a)Address of before instruction	
	b)Address of the next instruction	
	c)Data of the before execution to be executed	

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	d)Data of the execution instruction	
9	9.If we push data onto the stack then the stack pointer	1
	A)Increases with every push	
	b)decreases with every push	
	c)increases & decreases with every push	
	d)none of the mentioned	
10	10.How many bytes of bit addressable memory is present in 8051 based microcontrollers	1
	a)8 bytes	
	b)32 bytes	
	c)16 bytes	
	d)128 bytes	
	e)cant be determined	
11	11.JZ, JNZ, DJNZ, JC, JNC instructions monitor the bits of which register	1
	a)DPTR	
	b)B	
	c)A	
	d)Flag	
12	12.The ports act address lines	1
	a)PORT 0 and PORT 1	
	b)PORT 1 and PORT 2	
	c)PORT 0 and PORT 2	
	d)PORT 1 and PORT 3	
	e)CLR P0.05H	
13	13.Which addressing mode is used in pushing or popping any element on or from the stack	1
	a)Immediate	
	b)direct	
	c)indirect	
	d)register	
14	14.If SUBB A,R4 is executed, then actually what operation is being applied	1
	a)R4+A	
	b)R4-A	
	c)A-R4	
	d)R4+A	
15	15.Which instructions have no effect on the flags of PSW	1
	a)ANL	
	b)ORL	
	c)XRL	
	d)**All of the mentioned**	
16	16.TF1, TR1, TF0, TR0 bits are of which register	2

	a)TMOD	
	b)SCON	
	c)TCON	
	d)SMOD	
17	17.What steps are followed when we need to turn on any timer	2
	a)Load the count, start the timer, keep monitoring it, stop the timer	
	b)Load the TMOD register, load the count, start the timer, keep monitoring it, stop the timer	
	c)load the TMOD register, start the timer, load the count, keep monitoring it, stop the timer	
	d)none of the mentioned	
18	18.Auto reload mode is allowed in which mode of the timer	1
	a)Mode 0	
	b)Mode 1	
	c)Mode 2	
	d)Mode 3	
19	19.Which register is used to make the pulse a level or an edge triggered pulse	1
	a)TCON	
	b)IE	
	c)IPR	
	d)SCON	
20	20.What is the processor used by ARM7	1
	a)8-bit CISC	
	b)32-bit RISC	
	c)32-bit CISC	
21	21.What is the processor used by ARM7	1
	a)8-bit CISC	
	b)32-bit RISC	
	c)32-bit CISC	
22	22. ARM stands for	1
	a)Advanced RISC Machine	
	b)Advanced RISC Methadology	
	c)Advanced Reduced Machine	
	d)Advanced Reduced Methadology	
23	23.What is the instruction set used by ARM7	1
	a)16-bit instruction set	
	b)32-bit instruction set	
	c)64-bit instruction set	
	d)8-bit instruction set	
24	24.How is the nature of instruction size in CISC processors?	1
	a)Fixed	

	b)Variable	
	c)Both a and b	
	d)None of the above	
25	25.Abort mode generally enters when	2
	a)an attempt access memory fails	
	b)low priority interrupt is raised	
	c)ARM processor is on rest	
	d)ARM processor is on rest	
26	26.10.In a Cortex-A processor, which exception vector is located at the highest memory address of the exception vector table?	1
	a)Undefined Instruction	
	b)Data Abort	
	c)IRQ	
	d)FIQ	
27	27.The important feature of ARM is	1
	a)multi-tasking	
	b)Lower error	
	c)Efficient memory management	
	d)Low cost and low power consumption	
28	28.In the ARM Processor register R15 is a	1
	a)program counter	
	b)Stack Pointer	
	c)CPSR	
	d)SPSR	
29	29.MMU stands for	1
	a)Multiprocessor management unit	
	b)Memory management unit	
	c)Multi mode management unit	
30	30.GPIO stands for	1
	a**)General Purpose Input/Output**	
	b)Global Purpose Input/Output	
	c)none of them	
	d)General Public Input/Output	
31	31.The function of T0MCR is	
31	a)To increment on every clock	2
	b)Compare the values	
	c)After finding match controls the action	
	d)All above	
32	32.The function of IODIR is	2
	a)To set pins as either input or output pins.	
	b)To read or write values directly to the pin	

	c)To clear the values directly to the pin	
	d)None of above	
33	33.The function of TOPR	2
	a)To hold the maximum value of prescale counter	
	b)It continuously compares to the Timer Counter (TC) value.	
	c)It is incremented when the Prescale Counter (PC) reaches its maximum	
	d)All above	
34	34.LPC 2148 belongs to	2
	a)ARM7E940t	
	b)ARM7EJ-S	
	c)ARM720T	
	d)none of above	
35	35.What should be the value to be entered in the PWMCR REGISTER for single edge control of PWM3	2
	a)0x00000800	
	b)0x00000802	
	c)0x00000804	
	d)0x00000808	
36	36.Pulse Width Modulation is used to control	2
	a)The speed of motor	
	b)To control period and duty cycle of square wave	
	c)To control the light intensity of dimmer	
	d)All above	
37	37.LPC2148 has	2
	a)32kB on chip RAM and 128kB FLASH memory	
	b)IMB RAM and 512kB on chip FLASH memory	
	c)64kB RAM and 512kB on chip FLASH memory	
	d)None of above	
38	38.LPC 2148 has ..... I/O pins	1
	a)32	
	b)64	
	c)16	
	d)none of above	
39	39.The IOSET register is	2
	a)Register that controls the state of output pins	
	b)Register that configure I/O Pins	
	c)GPIO Port Output Set registers	
	d)All above	
40	40.CJNE instruction makes	2
	a) the pointer to jump if the values of the destination and the source address are equal	

	b) sets CY=1, if the contents of destination register is greater then that of the source register	
	c)sets CY=0, if the contents of destination register is smaller then that of the source register	
	d)none of the mentioned	